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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,458	06/10/2005	Lonnie Goff	US02 0598 US2	3872
65913	7550	05/29/2009		
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER MAMO, ELIAS	
			ART UNIT 2184	PAPER NUMBER
			NOTIFICATION DATE 05/29/2009	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

# Office Action Summary

**Application No.**

10/538,458

**Applicant(s)**

GOFF, LONNIE

**Examiner**

ELIAS MAMO

**Art Unit**

2184

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 March 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Objections***

**Claims 7-10** are objected to because of the following informalities: claims 7-10 recite "The apparatus of claim 6..." which appears to be mistyped, and it should read "The subsystem of claim 6..." Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 1-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (US 2003/0041205), hereinafter referred to as Wu.

Referring to **claim 1**, Wu teaches, as claimed, a method of performing configuration or control of a subsystem that includes multiple registers that define multiple configurations of the subsystem (i.e.-a method of configuring a USB compound device

that includes an address/endpoint management mechanism which defines multiple configurations according to the types of endpoints stored in the address/endpoint management mechanism, page 2, ¶ 21 and ¶ 23, lines 3-5), comprising: providing together with the subsystem a configuration/control unit having a controller portion (i.e.-microprocessor 510, page 4, ¶ 47 and page 3, ¶ 43, lines 3-5) and a read-only storage portion storing multiple sets of configuration data (Note: Wu innately teaches that the endpoint configuration mechanism 424 having a read only storage portion which stores configuration data, page 4, ¶ 47, lines 3-7), each of the sets of configuration data including configuration parameters for each of the multiple registers (page 4, ¶ 47, lines 4-5), and each of the sets of configuration data defining a respective one of the multiple configurations (Note: each of the saved configurations data defines one of the plurality of endpoint type stored in the address/endpoint management mechanism, page 2, ¶ 23, lines 3-9).

Further, Wu teaches that according to signals received from the USB link layer (page 3, ¶ 41, lines 2-3), the microprocessor 510 defines buffer blocks for each of end point devices and the buffer blocks are used as data register blocks in order to store the configuration data (page 4, ¶ 46). However, Wu does not explicitly teach where the configuration/control unit, in

response to a single register write that identifies one of the sets of configuration data, encapsulating the multiple registers by performing configuration or control of the subsystem, including storing the configuration parameters of the identified set in the multiple registers of the subsystem.

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Wu so that the configuration/control unit, in response to a single register write that identifies one of the sets of configuration data, encapsulating the multiple registers by performing configuration or control of the subsystem, including storing the configuration parameters of the identified set in the multiple registers of the subsystem, since such modification is merely an alternate arrangement which falls within the level of ordinary skill in the art. The motivation for doing so would have been design simplicity or convenience in order to gain the commonly understood benefits such as simplified operation.

As to **claim 2**, Wu teaches the method of claim 1, wherein the subsystem is a universal serial bus (USB) block, and the multiple configurations include Control mode, Interrupt mode, Isochronous mode, and Bulk mode (page 1, ¶ 7, lines 5-8), each

of the modes encapsulated by a single write to a common register location (Note: as discussed in claim 1 above, implementing a single write operation is an alternate arrangement), and wherein the subsystem is a hardware subsystem (i.e.-item 40, see fig. 4), and the configuration/control unit is a hardware configuration/control unit (see fig. 4).

As to **claim 3**, Wu teaches the method of claim 2, wherein the hardware subsystem and the hardware configuration/control unit are provided together within the same integrated circuit (page 2, ¶ 21 and see fig. 4).

As to **claim 4**, Wu innately teaches the method of claim 1 wherein the storing of the configuration parameters of the identified set in the multiple registers is implemented using a bus having a width sufficient to simultaneously store the configuration parameters of the identified set (page 7, ¶ 78, lines 1-4).

As to **claim 5**, Wu teaches the method of claim 1, wherein the configuration/control unit is responsive to multiple different values for the single register write for performing different corresponding configuration or control actions with respect to the subsystem, each of the different values identifying one of

the sets of configuration data (i.e.-identification information is used in order to define the transmission type, and also to determine one of the multiple functions connected to the compound device, page 4, ¶ 51).

Referring to **claim 6**, Wu teaches a subsystem having self-configuration capabilities (i.e.-item 40, see fig. 4), comprising: a register section including multiple registers that define multiple configurations of the subsystem (Note: the microprocessor 510 defines buffer blocks which are used as data register blocks in order to store multiple configuration data, page 4, ¶ 46); and a configuration/control unit having a controller portion (i.e.-microprocessor 510, page 4, ¶ 47 and page 3, ¶ 43, lines 3-5) and a read-only storage portion (Note: Wu innately teaches that the endpoint configuration mechanism 424 having a read only storage portion which stores configuration data, page 4, ¶ 47, lines 3-7) storing multiple sets of configuration data, each of the sets of configuration data including configuration parameters for each of the multiple registers (page 4, ¶ 47, lines 4-5), and each of the sets of configuration data defining a respective one of the multiple configurations (Note: each of the saved configurations data

defines one of the plurality of endpoint type stored in the address/endpoint management mechanism, page 2, ¶ 23, lines 3-9).

Further, Wu teaches that according to signals received from the USB link layer (page 3, ¶ 41, lines 2-3), the microprocessor 510 defines buffer blocks for each of end point devices and the buffer blocks are used as data register blocks in order to store the configuration data (page 4, ¶ 46). However, Wu does not explicitly teach wherein the configuration/control unit is configured, responsive to a single register write that identifies one of the sets of configuration data, to encapsulate the multiple registers by performing configuration or control of the subsystem, including storing the configuration parameters of the identified set in the multiple registers of the subsystem.

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Wu so that the configuration/control unit, in response to a single register write that identifies one of the sets of configuration data, encapsulating the multiple registers by performing configuration or control of the subsystem, including storing the configuration parameters of the identified set in the multiple registers of the subsystem, since such modification is merely an alternate arrangement which falls with



in the level of ordinary skill in the art. The motivation for doing so would have been design simplicity or convenience in order to gain the commonly understood benefits such as simplified operation.

As to **claim 7**, Wu teaches the apparatus of claim 6, wherein the subsystem is a universal serial bus (USB) block, and the multiple configurations include Control mode, Interrupt mode, Isochronous mode, and Bulk mode (page 1, ¶ 7, lines 5-8), each of the modes encapsulated by a single write to a common register location (Note: as discussed in claim 1 above, implementing a single write operation is an alternate arrangement), and wherein subsystem is a hardware subsystem (i.e.-item 40, see fig. 4), and the configuration/control unit is a hardware configuration/control unit (see fig. 4).

As to **claim 8**, Wu teaches the apparatus of claim 7 wherein the hardware subsystem and the hardware configuration/control unit are provided together within the same integrated circuit (page 2, ¶ 21 and see fig. 4).

As to **claim 9**, Wu innately teaches the apparatus of claim 6, further comprising a bus having a width sufficient to

simultaneously store the configuration parameters of the identified set in the multiple registers (page 7, ¶ 78, 1-4).

As to **claim 10**, Wu teaches the apparatus of claim 6, wherein the configuration/control unit is responsive to multiple different values for the single register write for performing different corresponding configuration or control actions with respect to the subsystem, each of the different values identifying one of the sets of configuration data (i.e.-identification information is used in order to define the transmission type, and also to determine one of the multiple functions connected to the compound device, page 4, ¶ 51).

Referring to **claim 11**, Wu teaches, as claimed, for use in a system that includes a processor coupled to a hardware subsystem via a system bus (i.e.-USB logic module 400 coupled with microprocessor 510, page 4, ¶ 47 and see fig. 4), the hardware subsystem including a configuration/control unit (endpoint configuration mechanism 424, see fig. 4) and a plurality of registers that define multiple configurations of the subsystem (Note: Wu innately teaches an endpoint configuration mechanism 424 having a read only storage portion which stores configuration data, page 4, ¶ 47, lines 3-7), a method of

configuring the subsystem comprising: storing a plurality of sets of configuration data in a read-only memory of the configuration/control unit (Note: Wu innately teaches an endpoint configuration mechanism 424 having a read only storage portion which stores configuration data, page 4, ¶ 47, lines 3-7), each of the sets of configuration data including configuration parameters for each of the plurality of registers (page 4, ¶ 47, lines 4-5),, and each of the sets of configuration data defining a respective one of the multiple configurations (Note: each of the saved configurations data defines one of the plurality of endpoint type stored in the address/endpoint management mechanism, page 2, ¶ 23, lines 3-9). Further, Wu teaches that according to signals received from the USB link layer (page 3, ¶ 41, lines 2-3), the microprocessor 510 defines buffer blocks for each of end point devices and the buffer blocks are used as data register blocks in order to store the configuration data (page 4, ¶ 46).

However, Wu does not explicitly teach, responsive to the configuration/control unit receiving, from the processor, a single register write that identifies one of the sets of configuration data encapsulating the plurality of registers by writing the configuration parameters of the identified set from the read-only memory of the plurality of registers.

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Wu so that responsive to the configuration/control unit receiving, from the processor, a single register write that identifies one of the sets of configuration data encapsulating the plurality of registers by writing the configuration parameters of the identified set from the read-only memory of the plurality of registers, since such modification is merely an alternate arrangement which falls within the level of ordinary skill in the art. The motivation for doing so would have been design simplicity or convenience in order to gain the commonly understood benefits such as simplified operation.

As to **claim 12**, Wu teaches the method of claim 11, wherein the configuration/control unit is a state machine (Note: the USB logic module 400 is comprised of generic endpoint state machine 421, see fig. 4).

As to **claim 13**, Wu teaches the method of claim 11, wherein the subsystem is a USB block comprising a plurality of ports that can operate in different modes (page 2, ¶ 19) responsive to which of the sets of configuration data is written to the plurality of registers (page 3, ¶ 42, lines 6-8).

As to **claim 14**, Wu innately teaches the method of claim 11, wherein the storing of the configuration parameters of the identified set in the plurality of registers is implemented using a bus having a width sufficient to simultaneously store the configuration parameters of the identified set (page 7, ¶ 78, lines 1-4).

As to **claim 15**, Wu teaches the method of claim 11, wherein the configuration/control unit is responsive to multiple different values for the single register write for performing different corresponding configuration or control actions with respect to the subsystem, each of the different values identifying one of the sets of configuration data (i.e.-identification information is used in order to define the transmission type, and also to determine one of the multiple functions connected to the compound device, page 4, ¶ 51).

### ***Response to Arguments***

Applicant's arguments filed on 03/12/2009 have been fully considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ELIAS MAMO whose telephone number is (571) 270-1726 and fax number (571) 270-2726. The examiner can normally be reached on Monday

thru Thursday from 9 AM to 5 PM EST. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai, can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/E. M./

Examiner, Art Unit 2184

**/Henry W.H. Tsai/  
Supervisory Patent Examiner, Art Unit 2184**